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Slip-Free Rapid Thermal Processing in Single Wafer Furnace

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Defect generation phenomena in Si wafers during atmospheric pressure rapid thermal processing (RTP) in a single wafer furnace (SWF) are investigated as a function of temperature, process time, wafer handling method and speed. The size, shape and spatial distribution of crystal defects generated during RTP were characterized using an optical microscope and X-ray topography. The wafer handling method and speed are found to be very important in controlling defect generation during RTP under given process conditions. Highly reproducible slip-free RTP results were achieved in 200-mm-diameter Si wafers processed at 1100°C for 60 s (up to 5 times) by optimizing the wafer handling method and speed.

KEYWORDS: single wafer furnace (SWF), rapid thermal processing (RTP), defect generation, slip, X-ray topography

1. Introduction

Single wafer, rapid thermal processing (RTP) technology has significant advantages over thermal processing in traditional batch furnaces (150–200 wafers/batch) in terms of thermal budget reduction and process flexibility improvement in temperature range and lot sizes.[1)] Typical furnace processing times ranged from 4–6 h per batch. High temperature processing times could approach 10 h per batch. Typical ramp-up and ramp-down rates in standard vertical furnaces are ∼10°C/min and ∼3°C/min, respectively.[2)] Typical processing times in an RTP system are 1–5 min per wafer, while the ramp-up and ramp-down rates range from 20°C/s to 250°C/s, respectively. Rapid wafer temperature ramping makes the thermal process very efficient without increasing the thermal budget.[3)] However, a small temperature gradient on wafers heated above 1000°C can cause plastic deformation (crystalline slips) which strongly affects the device yield.[4)] The slip-free RTP of large diameter (200 mm and above) Si wafers is still a significant technical challenge.[5)]

Typical cold-wall-type RTP systems employ halogen lamps to heat wafers by optical interaction between the light source (lamps) and the wafer. The hot-wall-type RTP system uses a resistively heated susceptor as a heat source. Lamp-based RTP systems have very poor energy efficiency and require complicated temperature measurement/control algorithms to maintain wafer temperature uniformity during processing and minimize temperature overshoot or undershoot. Although the susceptor-based RTP systems have higher energy efficiency, they can only be used in low-pressure (<100 Torr) nonoxidation environments due to the susceptor material (SiC-coated graphite), because of large heat loss from the susceptor to the water-cooled chamber wall through gas conduction.[6)]

To overcome the drawbacks of batch furnaces and single wafer RTP systems, we have designed a single wafer furnace (SWF) with a vacuum loadlock.[7)] In this study, defect generation phenomena in 200-mm-diameter Si wafers during RTP in a SWF are investigated as a function of temperature, pressure, processing time, wafer handling method and speed. The effects of each process parameter are characterized using an optical microscope and X-ray topography. A defect generation mechanism is proposed based on defect characterization results. Slip-free RTP process results after process parameter optimization are demonstrated.

2. Single Wafer Furnace

In the SWF system, the process chamber temperature is maintained at a predetermined temperature. Wafers are carried in and out of the preheated process chamber instead of controlling their temperature directly. The SWF process chamber consists of a transparent quartz reactor, a silicon carbide cavity, a heater assembly and an aluminum housing. Since the process chamber is made of quartz, the system can be used in oxidation as well as annealing applications. The process chamber has three standoffs made of quartz and no moving parts inside. The wafer is placed on the quartz standoffs (8–9 mm tall) in the middle of the process chamber. The distance between the wafer and the quartz walls is kept at ∼10 mm for both upward and downward directions. The quartz process chamber is located in a SiC cavity which acts as a heat distributor to create an isothermal processing environment. The SiC cavity is surrounded by a three zone heater assembly. The process chamber temperature is kept constant at a predetermined temperature. A nearly isothermal environment, where the wafer is processed, is created by the SiC cavity with very high thermal conductivity. Details of the process chamber are described in the previous report.[7)]

3. Experiment

Si wafers of 200-mm-diameter were annealed in the preheated process chamber in the temperature range of 800 to1150°C. Crystalline defects generated in the Si wafers during atmospheric pressure annealing are investigated by visual inspection and optical microscopy as a function of temperature, pressure, process time, wafer handling method and speed. A fixed unit processing time of 60 s was used. The total processing time was varied by repeating the 60 s unit process. Wafers were processed one to five times. Wafers without visible defects are characterized by X-ray topography. The size, shape and spatial distribution of crystal defects generated during RTP were characterized.

The wafer handling sequence is as follows: (1) the wafer handling robot picks up a wafer, (2) the process chamber gate valve opens, (3) the robot carries the wafer into the process chamber, (4) the robot lowers the wafer onto the standoffs, (5) the robot leaves the process chamber, (6) the gate valve

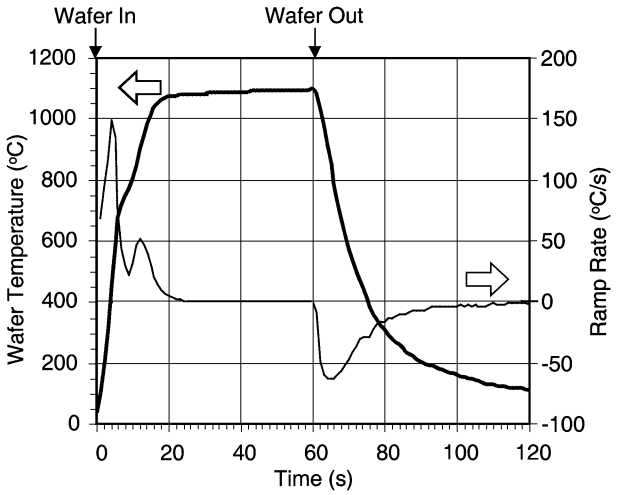

Fig. 1. Wafer temperature profile and ramp rate of 60 s process at 1100°C.

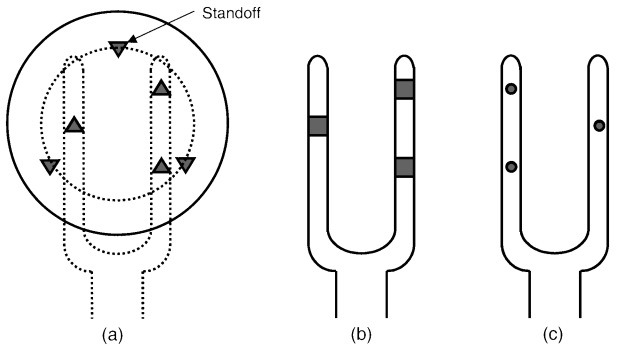

Fig. 2. Relative positions of contact area on 200-mm-diameter Si wafer (a) and schematic illustrations of end effectors (type A (b) and type B(c)).

closes, (7) the wafer remains in the process chamber for the given process time (8) the gate valve opens, (9) the robot goes into the process chamber, (10) the robot picks up the annealed wafer, (11) the robot removes the wafer from the process chamber at process temperature, (12) the gate valve closes, (13) the wafer cools down on the end effector of the robot by radiation and natural convection.

Figure 1 shows the temperature profile and ramp rate of a 200-mm-diameter Si wafer during ramping-up, processing and ramping-down. The furnace temperature and pressure were 1100°C and 760 Torr, respectively. The wafer temperature was measured using a very fine, bare, R-type (Pt-13% Rh/Pt) thermocouple bonded on the wafer. The wafer is heated as soon as it is placed in the preheated process chamber. The wafer temperature increases rapidly and approaches the process chamber temperature in less than 20 s. The initial ramp rate ranges from 70°C/s to 150°C/s at a furnace temperature of 1100°C. The wafer is quickly removed after processing, at almost the process temperature. Exponential ramping-down is observed during natural cool down step. Wafer cooling is normally done in a cooling station. The wafer temperature reaches 60°C in less than 60 s from the time of wafer retrieval at 1100°C when cooling is done in the cooling station.

4. Results and Discussion

Two types of end effectors were used in this study. The end effectors were made of clear quartz. One (type A) has three square pads (14 mm × 14 mm in area and 1 mm in height) and the other (type B) has three small rounded dots (∼3 mm in diameter and 1 mm in height). The purpose of using two different types of end effector is to investigate the size and shape effects of the contact points. The wafer touches three points (either three square pads or three dots) during wafer transfer to and from the process chamber. The wafer also touches the three quartz standoffs during annealing. The quartz standoffs are at furnace temperature. Figure 2 shows the relative positions of the contact areas on the 200-mm-diameter wafer and schematic illustrations of the two end effectors.

4.1 Wafer handling speed

The average wafer transfer (insert and removal) speed was varied between 100 mm/s and 400 mm/s. Wafers transferred at less than 200 mm/s showed some slip lines at temperatures above 1050°C even after a one time annealing for 60 s. Wafer pick-up and placement speeds between 0.5 mm/s and 16 mm/s did not show any difference under visual inspection. All the wafers transferred at more than 200 mm/s and processed once for 60 s in the temperature range of 800 to1150°C did not show any visual slips regardless of pressure and end-effector type. Wafers processed five times above 1050°C showed slip lines in the area where they came into contact with the end effector. The slip lines become longer as the process temperature and wafer pick-up speed increased during wafer retrival after processing. These trends can be explained as thermal and mechanical stress increases due to an increase in temperature difference between the wafer and the end effector and mechanical stress increase on the wafer backside during wafer-up. Gravitational stress due to the weight of the 200-mm-diameter Si wafer can cause slips above 1200°C if the weight is concentrated in a very small contact area.[5] During wafer placement in the process chamber, wafers make contact with standoffs far below the critical temperature for slip generation. No slip line was observed under any set of process conditions at the area where the wafer came into contact with the standoffs.

4.2 End effector type A

When wafers were transported by end effector A with three square pads and processed five times for 60 s periods each

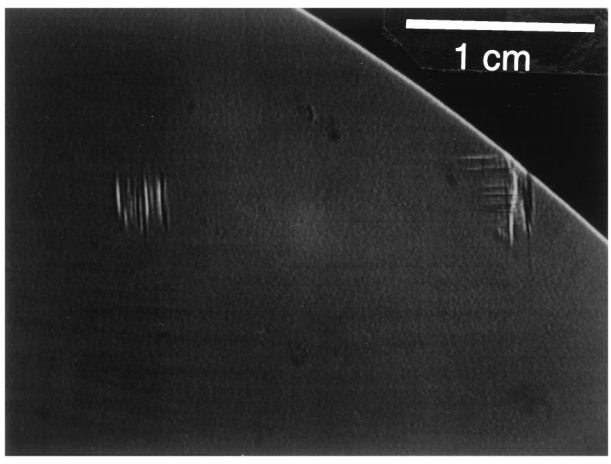

Fig. 3. Typical slip lines observed on wafers (1050°C, 60 s, 5 passes using effector type A).

at temperatures above 1050°C, they showed visual slip lines near the contact points along the [100] direction. The slip lines are longer when the process temperature is higher. Typical slip lines observed on wafers processed five times at temperatures above 1050°C are shown in Fig. 3. Slip lines were normally observed at the wafer edge and/or the area where the wafer came into contact with the three square pads on the end effector. Figure 4 shows time-elapsed wafer images during natural wafer cooling on the end effector with three square pads. The three dark areas on the wafer correspond to the three square pads on the end effector. When the cold end effector picks up the heated wafer, the contact areas lose heat to the end effector by conduction and radiation. This creates a large temperature gradient near the contact areas. Repeated thermal stress in the same area causes crystalline slips. Since crystalline slips can only occur above a critical temperature, uniform cooling of the wafer from the annealing temperature to the critical temperature is the key to preventing crystalline slip formation.

4.3 End effector type B

To reduce the thermal stress near the contact areas caused by heat loss from the wafer to the end effector, we have designed a new end effector with three small dots (Type B), to reduce the contact area and heat capacity of the contact points. Figure 5 shows time-elapsed wafer images during natural wafer cooling on the end effector with three small dots. Wafer cooling was done very uniformly. Three small dark spots start to appear as time passes. No slip lines were observed in the wafers processed five times for 60 s periods each in the temperature range of 800 to 1150°C under visual inspection and X-ray topography. Six small white spots corresponding to contact points with the three standoffs in furnace and the three dots on the end effector were observed in the X-ray topography image of a wafer annealed at 1100°C for 60 s. No slip lines were observed in wafers annealed five times at 1100°C for 60 s each. This result suggests excellent wafer temperature uniformity and excellent gravitational stress management even at high temperatures. The authors believe this rapid RTP technique in a SWF system can be applied to 300-mm-diameter Si wafers.

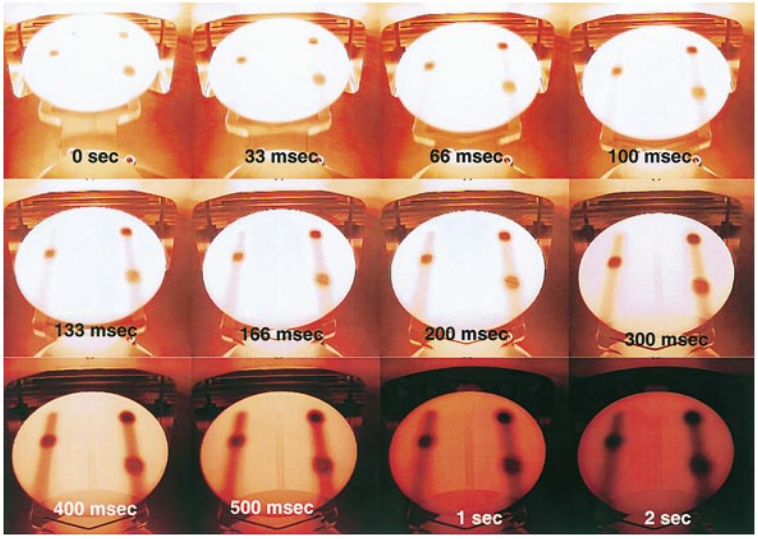

Fig. 4. Time elapsed wafer images during natural wafer cooling on the end effector with three square pads (type A).

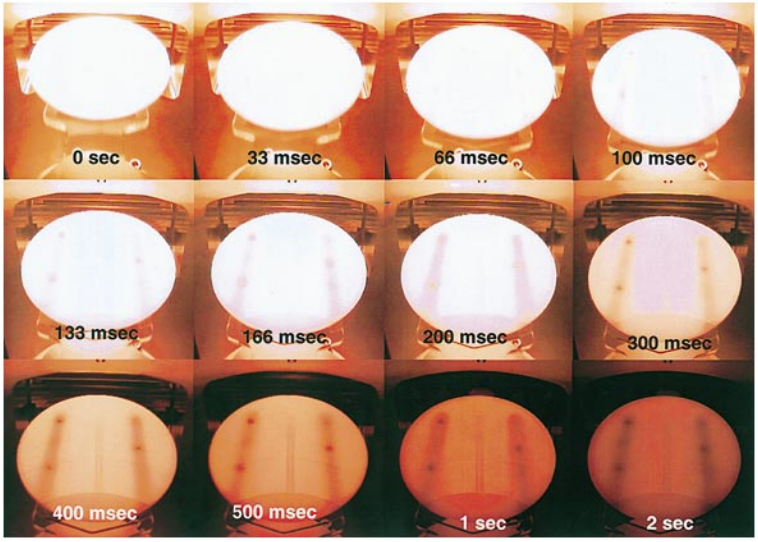

Fig. 5. Time elapsed wafer images during natural wafer cooling on the end effector with three small dots (type B).

5. Summary

Thermal behavior and defect generation phenomena in Si wafers during the atmospheric pressure RTP process in a SWF system are investigated as a function of temperature, process time, wafer handling method and speed. The size, shape and spatial distribution of crystal defects generated during RTP were characterized using an optical microscope and X-ray topography. The wafer handling method and speed are found to be very important in controlling defect generation during RTP under given process conditions. Highly reproducible slip-free RTP results were achieved in 200-mm-diameter Si wafers processed at 1100°C for 60 s (up to 5 times) by optimizing the wafer handling method and speed. The SWF system is very promising for RTP applications such as barrier-metal annealing, silicidation, oxidation, thin-film formation, glass densification, glass reflow, dopant diffusion, thermal donor annihilation and implant annealing up to 1150°C.

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